B³D-HPA Continuous-Field Photonic Chip Architecture with Physical Hash Addressing

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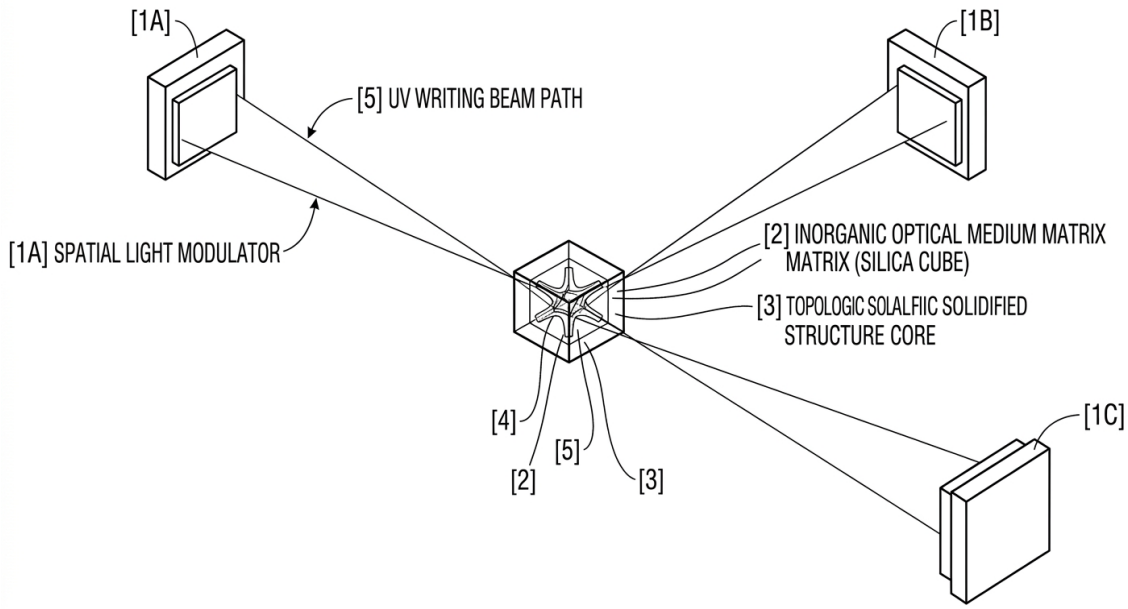
Abstract




The B³D-HPA architecture enforces a strict functional decoupling: Arithmetic Logic is strictly confined to the Geometric Polarization domain (Deterministic), while AI-driven regularization is offloaded to the Chaotic Phase domain (Probabilistic).

In this work, we introduce the B³D-HPA architecture. Embedding computational logic directly into fused silica materials is the first key breakthrough that turns continuous-wave optical computing from a theoretical concept into an engineering practical technology. Once this technical threshold is overcome, the future development path of continuous-wave optical computing will become completely clear and feasible.

We have built a complete EDA-compatible design method for the B³D-HPA architecture, which allows the entire optoelectronic system to be modeled and verified in standard industrial design tools from start to finish. We define the fused silica material as a parameterized static optical model, which has a fixed refractive index distribution and a physical hash anchor lattice made of rare-earth ions. The positions of these hash anchors and the logical connection paths between them can be easily built and simulated in standard photonic and electronic EDA software. The SLM control subsystem, UV pump drivers, and PD readout interface are designed as ordinary silicon-based circuits, so their timing coordination, signal synchronization, and signal stability can all be analyzed using standard EDA design processes.

A core upgrade in Version 3.51 is the launch of the PDMM Physical Dual-Modality Mapping Instruction Set (P-ISA). This is a physical-layer instruction framework completely different from traditional binary 0/1 encoding and coherent phase-locked photonic architectures. All EDA modeling and verification of this instruction set rely on intensity-based energy-level logic and relative physical parameters, which is consistent with the architecture's core design principle: a thermal-drift-immune deterministic skeleton and a chaotic semantic flow.

Unlike silicon instruction sets based on discrete 0/1 binary states or traditional photonic instruction sets relying on coherent phase control, this dual-modality instruction set uses wavelength as instruction, incoherent energy-level particle number changes, and controlled thermal drift as independent information-carrying dimensions. This technical change enables the creation of a real physical compiler directly implemented by the SLM array. This compiler can convert high-level user programs into physical hash anchor positioning, 3D energy-level gating control, and dual-modality light wavefield evolution.

All core computing operations—including intensity-based arithmetic calculations, incoherent energy competition, 3D gate superposition, and dual-modality wavefield evolution—can be accurately simulated and reproduced in photonic simulation software. This forms a complete closed engineering design path from defining physical dual-modality instructions to deploying final photonic computing, ensuring full predictability and formal traceability in the entire system operation process.

further completes the full system operation loop by officially defining the PDMM Physical Instruction Compiler (PIC) and the dual-mode working mechanism of the PD array, and fully establishing the complete PDMM P-ISA framework including deterministic basic instructions, chaotic basic instructions, and alignment normalization instructions.

The most prominent core feature is the full adoption of the PDMM Instruction Set, and in the incoherent deterministic instruction subset, geometric polarization subtractors, geometric polarization adders, thulium ion energy-level competition gain subtractors, and thulium ion energy-level adders are introduced as core computing units. Meanwhile, the phase deterministic computing part of previous versions is completely replaced by geometric polarization computing, and all phase operations are exclusively used for AI-oriented probabilistic computing instructions, realizing a fundamental reconstruction of the physical computing logic of the architecture.

The PD array has two key functions: it completes end-to-end logical meaning translation during computing inference, and provides closed-loop feedback to the SLM during recursive self-guiding writing or physical learning. Most importantly, the PDMM PIC realizes unified control of the SLM writing subsystem, PD readout subsystem, and lateral UV pump modulation drivers under a single instruction framework, enabling synchronous and coordinated writing, erasure, and dynamic 3D structure reconstruction. This unified

three-way closed-loop architecture allows the system to achieve real-time self-alignment and on-site physical learning without relying on complex high-dimensional inverse scattering calculations.

The core breakthrough is the verification of the natural spatiotemporal orthogonality between thulium ion-induced topological noise (S-Noise) and PD detector noise (P-Noise). This feature completely eliminates the risk of dual-modality instruction set failure caused by detector thermal drift.

S-Noise comes from the relaxation of thulium ion electron cloud orbits and energy-level fluctuations, with an atomic-scale spatial size (Å-level, 0.1 nanometers) and microsecond to millisecond (μs-ms) time scale; it acts as a controllable disturbance source for chaotic semantic flow. P-Noise comes from the thermal motion of semiconductor conduction/valence bands and shot noise inside the PD, with a nanometer to micrometer (nm-μm) spatial scale and picosecond (ps) time scale, which is uncorrelated random environmental interference.

The complete non-overlapping of spatial and temporal scales of these two noises enables automatic signal-noise separation at the physical layer without complex digital filtering algorithms, ensuring the absolute stability of PDMM dual-modality instruction execution in thermal drift environments.

Traditional silicon-based chips and memory-computing architectures rely heavily on process miniaturization and strict structural uniformity. As they approach physical manufacturing limits, they face insurmountable bottlenecks in power consumption, memory access walls, rising manufacturing costs, and yield rates.

A key industrial advantage of B³D-HPA is its ultra-high energy efficiency: compared with traditional silicon FP32 multiply-accumulators, the energy loss of optical interference computing is reduced by 3 to 4 orders of magnitude, providing an unparalleled efficiency advantage for large-scale deployment. 3D continuous-wave optical computing, with its natural parallelism, low light propagation loss, and wavefield interference computing capabilities, is regarded as a key development direction in the post-Moore era. However, inherent challenges such as material internal disorder, optical path instability, insufficient programmability, and lack of end-to-end encoding-decoding consistency have long restricted its practical industrial application.

This paper proposes the B³D-HPA (3D Body-High Performance Architecture), a continuous-wave optical computing architecture based on physical hash addressing. It uses rare-earth-doped fused silica as the core substrate, sapphire as an optional high-robustness material for extreme environments, and active-passive hybrid coherent phase lattices as distributed auxiliary reference structures. These phase lattices only provide limited spatial coordinate reference and auxiliary physical hash addressing (PHAT) initialization and fuzzy wavefield navigation, instead of global high-precision

phase locking.

This architecture takes light wavefield evolution and interference as the computing carrier. Through Physical Hash Mapping (PHM) and Physical Hash Address Tables (PHAT), it turns the inherent internal disorder of materials from a defect into a native computing resource. Instead of pursuing absolute material uniformity, it uses natural light scattering and refractive index distribution to achieve algorithm-level adaptive computing.

A core innovation of the architecture is the Recursive Physical Logic Probing (A*-based Self-Guiding Writing mechanism): it abandons the traditional coordinate-based path search method, and maps heuristic path guidance to optical wave propagation and fuzzy phase distribution. It realizes path exploration through probabilistic phase scanning, and locks effective path connections through energy-level trapping. This converts iterative digital search into closed-loop physical evolution, greatly reducing computing complexity and power consumption.

To support flexible and high-dimensional physical writing and parallel computing, the architecture introduces a customized laser input parallel array with geometric polarization rotation adjustment. Specially designed spatial light modulators (SLMs) are combined with artificially tailored polyhedral thulium nanoparticles with controllable polarization angles, enabling dynamic and precise writing of virtual waveguides inside the medium. Multiple SLM laser beams with distinct polarization angles can perform simultaneous independent information computing on the same thulium-based operator. Since polarization states can be designed to be mutually orthogonal, different optical computing channels do not interfere with each other, allowing direct high-dimensional information compression and large-model tensor mapping within a single physical volume. This multi-angle, multi-polarization parallel encoding mechanism significantly enhances the information density and computing throughput of the architecture, making it inherently suitable for large language models and high-dimensional artificial intelligence tasks.

To solve the problems of light diffraction spreading and signal-to-noise ratio (SNR) reduction, the architecture uses UV cold-writing technology to build a 3D gradient-index (GRIN) virtual waveguide network inside fused silica. According to Effective Medium Theory, rare-earth ions form a uniform effective medium instead of discrete scattering points, realizing boundaryless analog waveguides with low loss, natural matching with optical fibers, and dynamic reconfigurability. The self-focusing light distribution confines light within predefined topological paths, improving signal-to-noise ratio and mode stability.

At waveguide intersections, mode coupling and superposition occur, and optimal paths form strong output light peaks to complete the physical wavefield collapse. External light beams realize nanosecond-scale rapid reconfiguration, supporting on-site learning,

hardware evolution, and physical-level encryption.

retains the all-cold-state dual-level locking architecture, completely eliminating femtosecond laser structural ablation. Energy-level anchoring technology replaces physical material damage, fundamentally eliminating lattice damage inside the substrate.

For general GPU-equivalent general-purpose photonic acceleration scenarios, the architecture adopts a static or traditional reconfigurable topological form;
Only for autonomous AGI-oriented embodied intelligent scenarios, the architecture provides an optional reconfigurable bone-skin decoupling structure, which upgrades the hardware-software cooperation paradigm to a phylogeny-ontogeny evolutionary mechanism.

The architecture supports both fixed-structure GPU-like computing modes and evolutionary reconfigurable AGI modes, covering applications from general computing to high-adaptability intelligent systems.

B³D-HPA separates computing accuracy from physical material uniformity and absolute phase precision, allowing disordered materials to be used as reliable computing substrates. With dual-topology complementary robustness and the formally closed full instruction-compiler-execution-feedback loop, remaining technical challenges no longer constitute fundamental obstacles, providing a mass-producible, scalable, and practical development path for continuous-wave optical computing.

## 1 Introduction

Traditional digital computing relies on highly regular device structures and precise timing control. As manufacturing processes approach atomic scales, computing performance is restricted by thermal problems, interconnect delay, and manufacturing costs. Continuous-wave optical computing completes computing tasks through parallel propagation and interference of 3D light wavefields, with inherent advantages in low power consumption, high parallelism, and noise immunity. However, it has long been hindered by four practical technical barriers:

1. Internal material disorder and light scattering lead to non-reproducible computing results.
2. Optical path instability affects the consistency of computing results.
3. Weak programmability and reconfigurability limit its adaptation to real practical tasks.
4. Insufficient 3D light writing signal-to-noise ratio and processing speed restrict engineering implementation.

B³D-HPA abandons the pursuit of perfect material uniformity and global phase locking, and builds a technical framework centered on bounded fuzzy phase navigation, physical hash addressing, energy-level deterministic logic, and cross hybrid writing to ensure

reliability. Rare-earth phase lattices provide distributed on-site sensing and local reference signals. Physical hash addressing converts microscopic material variations into reusable physical fingerprints. Deterministic energy-level trapping ensures the stability of core computing logic. Multi-mode hybrid writing solves the long-standing signal-to-noise ratio and speed bottlenecks in 3D optical writing.

further strengthens the all-cold-state dual-level locking mechanism to replace femtosecond laser ablation, separating permanent computing backbone and dynamic modulation structures to completely eliminate physical material damage. By setting different energy locking depths, the system supports fully erasable, hybrid, and non-erasable working modes, greatly expanding its application scope.

For GPU-class general photonic computing, the bone-skin decoupling function is disabled, and the system maintains a stable fixed topological structure;
For advanced AGI-oriented scenarios, an optional reconfigurable bone-skin evolutionary decoupling mode is provided, enabling long-term adaptive evolution without human intervention.

A key technical insight refined in this version is the requirement of full-link consistency. In B³D-HPA, silicon-based clock synchronization is replaced by optical phase and address-space mapping synchronization. The input encoding protocol and PD output decoding protocol must be strictly aligned through a unified PHAT. Without such symmetrical consistency, even trillions-scale parallel wavefield evolution will only produce uninterpretable coherent noise.

The second core insight is the official definition of the PDMM Physical Instruction Compiler (PIC) running on the PDMM Physical Dual-Modality Mapping Instruction Set (P-ISA). PIC is a high-level compiler that runs on traditional silicon binary computing platforms, but it generates physical dual-modality optical instructions instead of traditional machine code. It directly programs the SLM to realize 3D wavefront modulation, the PD to complete output sampling or closed-loop feedback, and the UV pump drivers to realize lateral erasure and cross-locking writing, forming a complete end-to-end programming framework.

The third key insight is that the PDMM P-ISA is inherently compatible with large language models (LLMs) and deep neural networks. Its dual-modality encoding can naturally represent tensor structures, contextual embeddings, and high-dimensional semantic features, enabling direct physical-level parallel processing of large-model computing tasks without layer-by-layer digital simulation.

The fourth engineering insight is the instruction priority hierarchy based on physical robustness. The system prioritizes physical dimensions with natural thermal immunity (light intensity, wavelength anchoring) as the underlying core logic, and uses controlled phase drift as an advanced computing dimension, ensuring stable core logic operation in

conventional industrial environments.

The fifth pivotal physical insight is the spatiotemporal scale orthogonality of dual noise sources, which solves the core risk of PD thermal drift destroying the dual-modality instruction set. The inherent physical differences between thulium ion S-Noise and PD P-Noise form a natural physical filtering mechanism, eliminating the need for active algorithmic denoising, and ensuring that the chaotic semantic flow driven by S-Noise will not be disturbed by P-Noise, thus safeguarding the integrity of PDMM dual-modality mapping.

Final Goal

To realize mass-producible, stably operating, dynamically upgradable continuous-wave optical computing chips in non-laboratory industrial environments. The second-generation chip will not be designed by humans; it will be formed by the adaptive self-evolution of the first-generation chip in response to natural environmental conditions.

The first-generation B³D-HPA is not just a static photonic circuit; it is a "living" optical field. When deployed in real practical environments, it continuously interacts with external signal noise and mechanical disturbances. These environmental factors drive the system to find more stable, resilient, and energy-efficient light interference patterns and topological structures.

Therefore, the "second-generation" chip is not designed by human engineers, but is the natural result of this environmental adaptation. It is the architecture itself, which has learned to operate stably and efficiently in real environments, evolving into its next iteration.

In this technical paradigm, the role of human designers changes from "chip designer" to "seed planter". We define the basic rules of coherence, stability, and performance, and then let the system evolve according to physical laws and environmental requirements. The evolved chip generations are not limited by human imagination; they are shaped by the optimal solutions found by the light field itself.

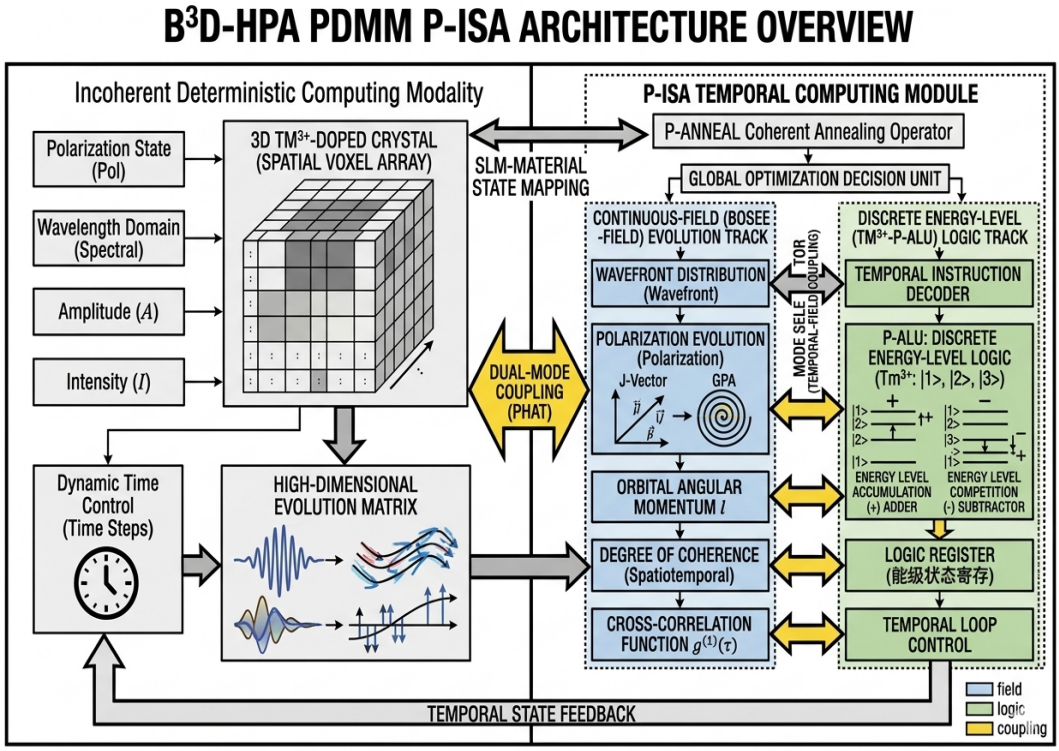
2 Fundamentals of Continuous-Wave Optical Computing and 3D Media

The computing power of continuous-wave optical computing comes from the coherent propagation and interference of 3D continuous light fields inside doped materials. Light amplitude, phase, wavelength, and polarization together define the global electromagnetic field state. Multi-path light superposition, mode coupling, and phase modulation jointly realize tensor-like parallel computing operations.

Different from discrete gate-level digital circuits, continuous-wave optical computing is fully parallel, clock-free, and requires no data movement between memory and

computing units, with fundamental advantages in communication bandwidth and energy efficiency.

2.0 PDMM Physical Dual-Modality Mapping Instruction Set (P-ISA)




The purpose of launching the PDMM P-ISA is to abstract the complex underlying physical light evolution process into predictable logical instructions. It is not only designed for programming, but also for establishing a rigorous mapping relationship from computing functions to hardware implementation in the EDA environment.

PDMM P-ISA (Physical Dual-Modality Mapping Instruction Set) is a universal computing framework that treats two physically orthogonal light-matter interaction modes as a unified instruction space:

- Modality I: Deterministic Skeleton – Based on incoherent energy-level particle number changes and intensity-gated logic, with natural immunity to thermal drift; core arithmetic operations are implemented by geometric polarization adders/subtractors and thulium ion energy-level adders/competition gain subtractors.
- Modality II: Chaotic Semantic Flow – Based on bounded fuzzy phase distribution and controlled physical disturbance, realizing probabilistic reasoning computing; all phase operations are exclusively applied to AI probabilistic computing instructions.

A defining feature of this instruction set is wavelength-as-instruction: each computing operation is directly addressed by a specific pump wavelength corresponding to the rare-earth ion resonance, eliminating the need for centralized instruction decoders and global clock signals.

Unlike traditional instruction sets (x86, ARM, RISC-V) that rely on serialized binary state transitions and 2D electronic circuits, PDMM P-ISA is designed for 3D photonic lattices and 3D optical computing media such as the B³D-HPA architecture. It encodes information and computing operations directly into 3D energy states and light wavefields, achieving massive parallelism without clock synchronization or memory data movement.

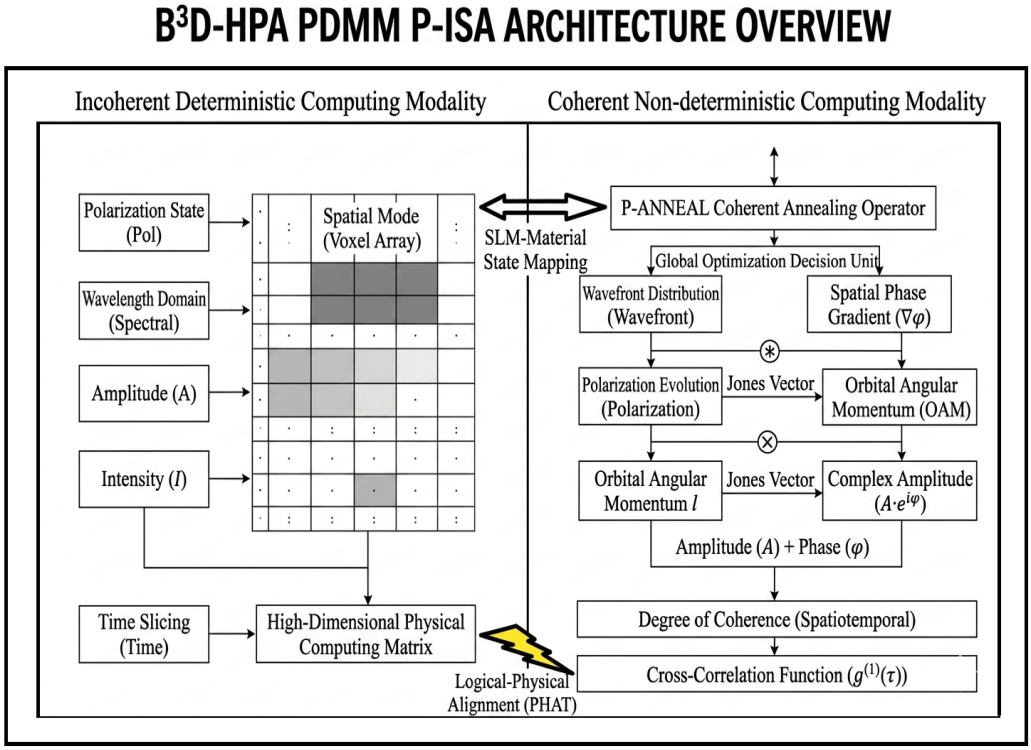
This instruction set is inherently suitable for large language models and high-dimensional AI computing tasks. Deterministic intensity logic (realized by polarization and thulium ion energy-level computing units) provides stable structural support, while chaotic phase interference can naturally represent word embeddings, attention mechanisms, tensor contractions, and contextual semantic representations, allowing LLMs to run directly through physical light wavefield evolution instead of digital matrix multiplication operations.

The core of LLM computing lies in high-dimensional embedding vectors, often with thousands of dimensions. In traditional binary electronic hardware, these high-dimensional structures are forced to undergo dimensionality reduction: they must be split, serialized, and transmitted through narrow computing pipelines. Under the PDMM P-ISA, light beams and 3D energy lattices can naturally carry high-dimensional structural information without conversion, and the physical representation is completely consistent with LLM tensor structures.

The most energy-intensive operation in LLMs—Self-Attention—essentially calculates the contextual relevance between text tokens. On GPU systems, this requires billions of iterative multiply-accumulate operations. Inside a 3D photonic computing medium, the relevance directly corresponds to the light wavefield coherence and interference strength supported by the deterministic energy-level skeleton. When two semantically encoded light wavefronts overlap in the lattice, their spatial interference pattern naturally encodes the attention score.

Text generation in LLMs is an autoregressive process, requiring long-term retention of past contextual states. Traditional architectures face catastrophic memory bottlenecks as context length increases. PDMM P-ISA uses the 3D spatial freedom inside the photonic medium to store these states as long-lived metastable energy-level patterns distributed across the computing volume, weaving these states directly into the 3D lattice instead of storing them in discrete memory units.

The instruction set does not require complex upfront design. A simplified basic version is sufficient for initial EDA verification, system startup, and self-guiding writing. Different manufacturers can independently develop extended instructions while maintaining compatibility with the core dual-modality framework, forming an open and independent industrial ecosystem.




2.0.0 Core Computing Units and Physical Formulas of Incoherent Deterministic Instruction Subset

Heterogeneous Deterministic Computing Paradigm
The B³D-HPA instruction set features a dual-domain deterministic execution model, bifurcating arithmetic operations into spatial-evolutionary and temporal-sequential modes:

Spatial-Evolutionary Domain (GPA): Implemented via Geometric Polarization Arithmetic, providing O(1) latency for massive tensor operations. It treats the 3D photonic medium as a continuous state-evolution field.

Temporal-Sequential Domain (Thulium Energy-Level Logic): Implemented via $Tm^{3+}$ cross-relaxation competition, functioning as a high-speed physical register queue. It provides deterministic sequential state updates, essential for autoregressive tasks.

2.0.0.1 Geometric Polarization Computing Units

The Jones vector framework is deployed within the chaotic semantic domain (Modality II), enabling the hardware to treat polarization-state evolution as a native probabilistic regularizer for high-dimensional tensor mapping, fundamentally decoupling computational logic from phase-locking sensitivity.

Mathematical Verification of Geometric Polarization Arithmetic (GPA)

The GPA operates on the basis of Jones Vector projection. For two input channels with Jones vectors J1 and J2 and an relative polarization angle Δθ, the logic gates are governed by the following analytical model

1.Geometric Polarization Adder (GPA-Add):

$I_{out} = J1^{\dagger}J1 + J2^{\dagger}J2 + 2|J1||J2|\cos(\Delta\theta)$

Logic Note: When $\Delta\theta \rightarrow 0$, the constructive intensity summation maximizes the logical state. This ensures that the adder is inherently immune to phase-induced destructive interference.

2.Geometric Polarization Subtractor (GPA-Sub):

$I_{out} = | J1^{\dagger}J1 - J2^{\dagger}J2 | \cdot \sin^2(\Delta\theta)$

Logic Note: By setting $\Delta\theta = \pi/2$ (orthogonal state), the subtraction operation achieves a null-point suppression, effectively implementing a physical-layer XOR logic.

The phase deterministic computing module of previous versions is completely replaced by geometric polarization adders and subtractors, which realize deterministic intensity arithmetic based on polarization state manipulation, completely immune to thermal drift and coherent interference noise.

1. Geometric Polarization Adder

Physical Formula:

$I_{out}^{add} = I_1 + I_2 - 2\sqrt{(I_1 I_2)}\cos\Delta\theta_{pol}$

Where $I_{out}^{add}$ is the output light intensity after polarization addition, $I_1$ and $I_2$ are the input light intensities of two optical paths, $\Delta\theta_{pol}$ is the geometric polarization angle difference between the two input light beams, and the operation realizes incoherent intensity superposition based on polarization state regulation.

2. Geometric Polarization Subtractor

Physical Formula:

$I_{out}^{sub} = |I_1 - I_2 + 2\sqrt{(I_1 I_2)}\cos\Delta\theta_{pol}|$

Where $I_{out}^{sub}$ is the output light intensity after polarization subtraction, and the geometric polarization angle difference $\Delta\theta_{pol}$ is precisely modulated to realize accurate incoherent light intensity difference calculation.

The intensity-based physical formulas represent the projection of the Jones space arithmetic onto the incoherent detection domain, where the polarization angle $\Delta\theta_{pol}$ acts as the control parameter for the physical compiler (PIC).

Geometric Polarization Based Fourier Transform Module

The geometric polarization arithmetic replaces phase-locked computation to realize Fourier transform operations in the incoherent intensity domain.

A polarization-controlled Fourier transform engine is constructed using Jones vector projection and polarization angle modulation, which is naturally immune to thermal drift and coherent noise.

Physical Definition of GPA-Fourier Transform

For an input light field with spatial distribution I(x,y) and polarization state parameter θ(x,y), the one-dimensional geometric polarization Fourier transform is defined as:

$$GF(k) = \int I(x) \cdot \cos( \Delta\theta_{pol}(x) - 2\pi kx ) \, dx$$

where
GF(k) represents the geometric polarization Fourier spectrum,
I(x) is the input incoherent light intensity distribution,
$\Delta\theta_{pol}(x)$ is the geometric polarization angle difference along the spatial dimension,
k is the spatial frequency component.

Physical Realization in B³D-HPA

The SLM array imposes a linear polarization angle gradient along the spatial dimension of the light field.
Interference between orthogonal polarization components performs coherent-like summation within the incoherent intensity domain.
The PD array detects the integrated intensity output to obtain the Fourier spectrum directly without global phase locking or complex phase stabilization.

Key Advantages

1. The Fourier transform is realized using geometric polarization rather than pure phase control.
2. The operation remains deterministic under thermal drift and environmental disturbance.
3. It supports parallel volumetric Fourier transform inside the 3D photonic medium.
4. It can be cascaded with geometric polarization adders and subtractors to form a complete signal processing pipeline.

2.0.0.2 Thulium Ion Energy-Level Computing Units

Based on the energy-level transition and cross relaxation characteristics of thulium ions in fused silica matrix, energy-level adders and competition gain subtractors are constructed to realize deterministic energy-level arithmetic operations.

1. Thulium Ion Energy-Level Adder
Physical Formula:
$N_{total} = N_1 + N_2 - N_{non\text{-}rad}$
Where $N_{total}$ is the total particle number of excited thulium ions after addition, $N_1$ and $N_2$ are the excited particle numbers of the two input energy levels, $N_{non\text{-}rad}$ is the

non-radiative relaxation loss particle number, and the operation realizes excited particle number superposition through stimulated emission synergy.

Thulium-Ion Sequential Gain Control (Temporal Mode)
Unlike the spatial-mode GPA, the $Tm^{3+}$ energy-level competition operates in a temporal queue, defined by the rate equation:
$dN_{ex}/dt = R_{pump} - \sum N_{ex}/\tau_{rad} - \Gamma_{cross}(N_{ex}^2)$
Where $\Gamma_{cross}$ represents the cross-relaxation depletion rate. This mechanism acts as a physical-layer FIFO buffer, enabling deterministic sequential arithmetic in the incoherent instruction subset.

2. Thulium Ion Energy-Level Competition Gain Subtractor
Physical Formula:
$N_{res} = N_{max} \cdot \exp(-\Delta E_{comp}/(kT)) - N_{dep}$
Where $N_{res}$ is the residual excited particle number after subtraction, $N_{max}$ is the initial maximum excited particle number, $\Delta E_{comp}$ is the energy level competition difference, k is the Boltzmann constant, T is the ambient temperature, $N_{dep}$ is the particle number depleted by cross relaxation, and the operation realizes precise gain subtraction through energy-level competition and cross relaxation depletion.

2.0.1 PDMM Physical Instruction Compiler (PIC)

The PDMM Physical Instruction Compiler (PIC) is a dedicated software compiler for the PDMM P-ISA. It runs on standard silicon-based binary computing platforms but does not generate traditional binary machine code. Instead, it directly converts high-level user programs into PDMM dual-modality optical instructions for SLM programming, PD configuration, and synchronized UV pump driver control.

PIC acts as a unified interpreter between human-defined logical tasks and physical photonic computing execution. It parses tensor operations, attention heads, and context windows in high-level programs, and decomposes them into deterministic intensity-gated (polarization/energy-level) and chaotic phase-evolution instruction pairs without serialization or binary conversion. It does not perform complex full-wave optical inversion or holographic reconstruction; it only defines input light modulation rules, output signal sampling rules, and UV lateral pump timing sequences, allowing the light wavefield to complete computing tasks autonomously inside the material.

2.0.2 Input and Output Pumping Mechanism

The input pump uses wavelength-multiplexed optical pulses to continuously inject token embeddings and key-value (KV) states into the 3D photonic lattice without blocking. It uses WDM optical frequency combs to load multi-wavelength vector groups in parallel, mapping each logical operation to a special pump wavelength matched with geometric polarization modulation or thulium ion energy-level resonance.

The output pump collects light interference patterns and 3D energy-state distributions from the material through multi-channel spatial detectors and wavelength-resolved readout arrays. It converts the high-dimensional optical field back into text token logits and probability distributions through PD-based intensity detection and mode demultiplexing.

A real-time calibration loop compensates for mode cross-coupling problems. The PIC dynamically adjusts injection wavelengths, polarization angles and energy-level bias voltages to maintain clear deterministic logic boundaries, ensuring long-term stable operation for continuous AGI computing tasks.

2.0.3 SLM as Physical Compiler

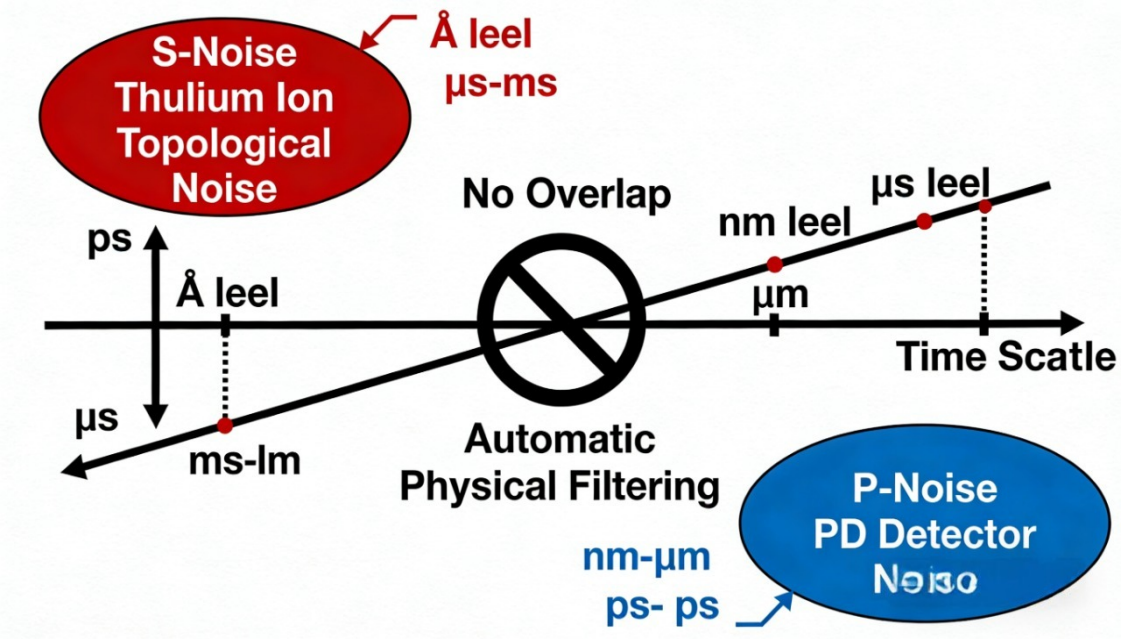
The SLM is not a display device; it is a real-time Physical Instruction Compiler (PIC). It translates high-level logical intent into 3D light-wavefield topology, transforming the $B^3D$-HPA substrate from a passive material into an active computational machine.

The SLM array acts as the physical compiler of the architecture, executing PDMM P-ISA instructions sent by the PIC. Its core functions are:

1. Accept dual-modality optical instructions from the PIC;
2. Directly convert logical instructions into wavelength-addressable physical operations including geometric polarization modulation and thulium ion energy-level excitation;
3. Generate 3D semantic navigation light patterns;
4. Bind logical computing nodes to physical hash anchors (PHAT);
5. Start recursive self-guiding light propagation or UV writing under synchronous timing with lateral pump beams.

The SLM does not perform full holographic reconstruction or pixel-level light path routing. It only provides logical task objectives and spatial navigation guidance, allowing the light wavefield to autonomously evolve into the optimal computing path inside the material. This fundamentally avoids the computing inversion bottleneck that has long restricted large-scale optical computing.

2.0.4 PD Array Dual-Mode Mechanism




Phase-based Semantic Denoising (AI-Oriented "De-firing")

While phase calculations are non-deterministic, they serve a critical role in AI-oriented probabilistic reasoning. We define this as the Phase-induced Entropy Shaping (PES) process:

$\Psi_{out} = \int_{Space} \exp(i \cdot \varphi(\vec{r}, t)) \cdot S_{semantic}(\vec{r}) \, d\vec{r}$

Where $\varphi(\vec{r}, t)$ is the chaotic phase distribution generated by the SLM. This process does not compute logic; rather, it performs a high-dimensional spatial smoothing of the semantic flow. By introducing controlled phase uncertainty, we allow the PD array to naturally "de-fire" (suppress over-fitting) in deep neural network inference, acting as a native physical-layer regularization.

The photodetector (PD) array operates in two complementary modes defined by the PIC and PDMM P-ISA, closing the entire physical computing loop:

Mode A: Inference Mode – Semantic Output Translation

During forward computing inference, the PD array acts as a semantic translator:

- The PD captures the output light intensity patterns and mode energy distributions generated by polarization/energy-level computing units;
- The PIC interprets the spatial-wavelength distribution through the PDMM P-ISA;
- The compiler maps physical light features into machine-interpretable digital outputs;
- Raw photonic signals are converted into structured results such as text, tensors, classification labels, or decision vectors.

Mode B: Training / Writing Mode – Closed-Loop Feedback to SLM

During self-guiding writing, physical weight embedding, or LLM training, the PD array acts as a feedback sensor:

- The PD detects real-time energy-level occupancy, polarization state and light interference accuracy;
- Measurement data is fed back to the PIC;
- The PIC updates PDMM instructions to adjust the SLM wavefront, polarization angle and UV pump intensity;
- The SLM dynamically guides the light wavefield to target physical hash anchors;
- This closed-loop mechanism realizes self-alignment and on-site physical learning without digital inverse scattering calculations.

Core Physical Optimization: Spatiotemporal Orthogonal Noise Screening
A fundamental enhancement of the PD dual-mode mechanism is the use of the natural spatiotemporal scale orthogonality between thulium ion topological noise (S-Noise) and PD electronic noise (P-Noise) to achieve automatic signal purification.

S-Noise comes from the internal electron cloud orbital relaxation and energy-level fluctuations of thulium ions, with an Å-level spatial scale and μs-ms temporal scale. It carries the topological information of the light field and acts as a legal driving source for chaotic semantic flow.

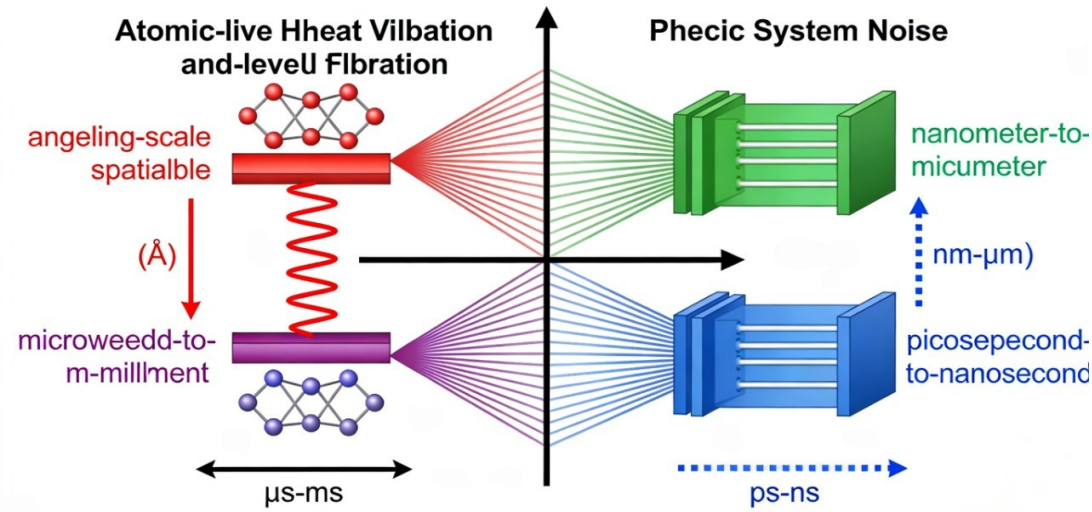
P-Noise is generated by the thermal motion and carrier fluctuation in the semiconductor conduction/valence bands of the PD, with a nm-μm spatial scale and ps-level temporal scale. It presents isotropic, uncorrelated random interference characteristics.

These two noise sources are completely orthogonal in the spatial and temporal domains with no overlapping frequency bands. During PD signal sampling, the system realizes physical-layer noise separation through inherent time integration and spatial manifold projection: ps-level high-frequency P-Noise is automatically averaged and filtered by the μs-ms sampling window matching S-Noise, and nm-μm scale uncorrelated P-Noise is filtered out by the Å-level topological correlation screening of the physical hash anchor lattice.

This mechanism eliminates the need for complex digital filtering algorithms, fundamentally preventing PD thermal drift and electronic noise from interfering with dual-modality instruction mapping logic, and ensuring stable operation of the PDMM instruction set in variable temperature environments.

Unified Spatiotemporal Orthogonality Constraint:
To ensure the integrity of the PDMM P-ISA, the system must satisfy the scale-separation inequality:
$\tau_{P\text{-}Noise} / \tau_{S\text{-}Noise} \ll 1 \quad \text{and} \quad \Lambda_{P\text{-}Noise} / \Lambda_{S\text{-}Noise} \gg 1$
Where $\tau$ denotes the temporal scale and $\Lambda$ denotes the spatial scale. This guarantees that deterministic skeleton logic (S-Noise dominated) remains protected from environmental PD interference (P-Noise dominated) without active digital filtering.

2.0.5 Orthogonal Noise Suppression: A Fundamental Physical Mechanism for Robust Photonic Computing



Orthogonal Noise Suppression in PDMM Architecture

A critical and industry-relevant physical mechanism embedded in the PDMM architecture is orthogonal noise suppression, derived from the inherent spatio-temporal scale separation between distinct physical origins of fluctuations.

Thermal vibrations, atomic-level energy-level fluctuations, and local lattice perturbations within thulium-doped media occur at characteristic angstrom-scale spatial displacements and microsecond-to-millisecond temporal scales.

In contrast, unwanted optical-electronic noise—including propagation scattering, detector readout noise, and mode jitter—exhibits nanometer-to-micrometer spatial scales and picosecond-scale temporal dynamics.

These two classes of disturbance occupy physically orthogonal domains, enabling natural, passive separation of computational signals from noise without complex active stabilization, active feedback, or precision temperature control.

This mechanism is not a minor engineering tweak, but a foundational physical property that resolves a long-standing bottleneck in practical photonic computing: environmental sensitivity and scalability barriers.

By exploiting orthogonal noise characteristics, PDMM achieves robust, repeatable computation in ambient conditions, eliminating the need for ultra-stable laboratories, complex isolation systems, and cryogenic cooling that have constrained conventional coherent photonic architectures to laboratory settings.

The orthogonal suppression principle thus enables reliable deployment of volumetric photonic hardware in real-world environments, drastically lowering manufacturing and operational costs while strengthening stability.

In this framework, noise is no longer an error source to be eliminated, but a physically bounded, scale-separable component that supports stochastic computing and natural annealing, further reinforcing the architectural robustness and industrial viability of PDMM.

### 2.0.6 Computable Geometric Polarization & Massively Parallel Deterministic Writing

A defining physical breakthrough of B³D-HPA is the strict computability of the geometric polarization response within thulium-doped fused silica. Since the local geometric polarization angle $\Delta\theta_{pol}$ can be directly determined by the population distribution of thulium energy levels under optical pumping, the polarization state at any spatial voxel (x,y,z) becomes a numerically predictable physical quantity rather than an uncertain or empirically calibrated parameter. This computability enables a paradigm shift in large-scale 3D optical programming: from iterative recursive self-guiding exploration to deterministic, single-shot holographic field mapping.

In contrast to recursive self-guiding writing, which relies on wavefield evolution, thermal-drift-driven physical annealing, and energy-level trapping to construct computational topologies, massively parallel deterministic writing directly precomputes the global geometric polarization distribution required by the target algorithm or neural network. The PDMM Physical Instruction Compiler (PIC) translates tensor operations, linear algebra transforms, and high-dimensional AI computational graphs into a spatially continuous polarization matrix, which is then imposed onto the thulium-doped medium via the SLM array in a single exposure step. Each pixel of the SLM corresponds to a programmable local polarization orientation, which is permanently or semi-permanently registered by the energy-level response of thulium ions, forming a virtual 3D computational waveguide network without discrete etching or layered fabrication.

This mechanism establishes a dual-mode programming architecture that defines the core industrial scalability of B³D-HPA:

#### 2.0.6.1 Skeleton Layer: Deterministic Holographic Writing for Massive Parallelism

The skeleton layer represents the fixed computational backbone of the architecture, programmed through deterministic holographic polarization mapping. It supports computationally stable workloads including matrix multiplication, Fourier transformation, convolution, tensor contraction, and large-model embedding operations. By precomputing the global Jones matrix distribution and geometric polarization angle layout, the system can instantiate an entire high-throughput computational engine in one optical exposure, eliminating the time cost of iterative self-guiding exploration. This approach is inherently optimized for GPU-equivalent general-purpose photonic acceleration, where fixed computational structures yield high energy efficiency, throughput, and reproducibility.

#### 2.0.6.2 Skin Layer: Chaotic Self-Guided Writing for Adaptive AGI Learning

The skin layer supports dynamic, on-site physical learning and adaptive topological evolution driven by controlled thermal drift and S-Noise. It operates on top of the stable skeleton layer and performs localized wavefield exploration, energy-level trapping, and

real-time PD feedback to refine computational paths, adjust synaptic weights, or optimize structural resilience. This mode is reserved for autonomous AGI and embodied intelligence scenarios, enabling long-term environmental adaptation without full reconfiguration of the entire computational medium.

2.0.6.3 Orthogonal Polaristic Multiplexing & Scalability

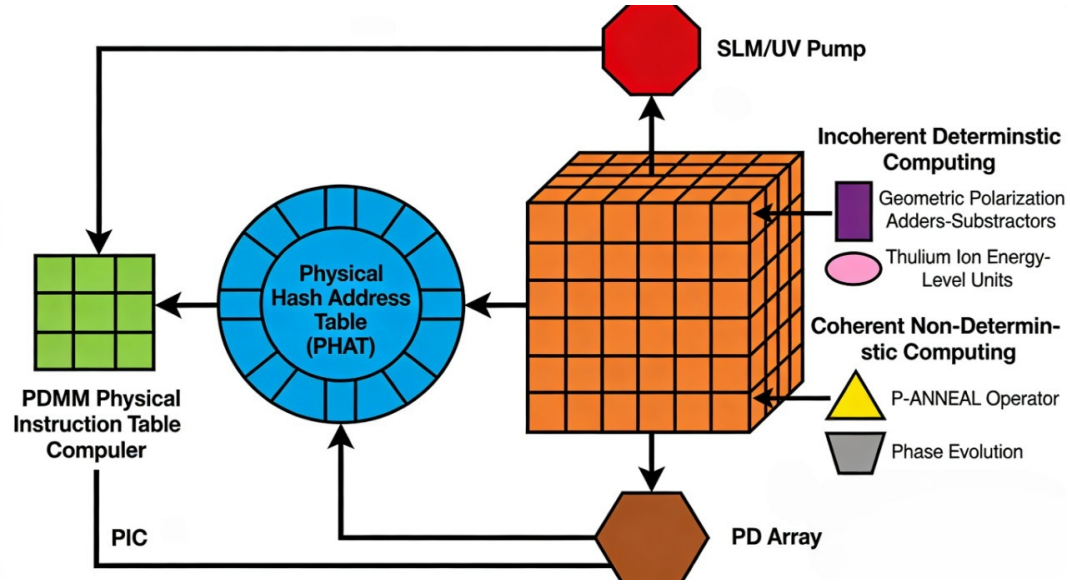
Massively parallel writing benefits fundamentally from the orthogonality of geometric polarization states. Multiple independent computational channels can be overlaid within the same physical volume using orthogonal polarization bases (0°, 90°, 45°, −45°), without mutual interference or cross-coupling. This allows the architecture to achieve ultra-high computational density by multiplexing logical layers within the 3D bulk medium, rather than relying solely on planar scaling. Combined with the atomic-scale spatial locality of thulium energy-level response, this enables computational integration densities comparable to or exceeding advanced sub-2nm semiconductor nodes, without facing the same thermal, interconnect, and fabrication bottlenecks.

2.0.6.4 Industrial Paradigm Shift: From Lithographic Etching to Holographic Computation Printing

The computability of geometric polarization and single-shot holographic writing fundamentally redefines the manufacturing model for photonic computing chips. Instead of subtractive lithography, deposition, and multi-layer stacking, the B³D-HPA platform uses optical field projection to “print” complete computational circuits directly into thulium-doped quartz wafers. Design updates require only a modified holographic polarization matrix file, eliminating expensive mask reconfiguration and tape-out costs. This allows decentralized, on-demand fabrication of photonic computing hardware using standardized optical writing systems, establishing a scalable, low-cost industrial path for post-Moore computing hardware.

In summary, deterministic computable geometric polarization writing enables the B³D-HPA architecture to achieve both massive throughput for general-purpose computing and adaptive learning for AGI systems. It removes the fundamental speed bottleneck of recursive physical probing while preserving the architecture’s unique ability to self-optimize in unstructured environments, forming a complete and industrially viable foundation for next-generation continuous-wave optical computing.

2.0.7 Full Workflow: Human Program to Physical Computation




The complete system operation chain is:

1. Humans provide high-level programs or LLM model logic;
2. The PIC compiles the input into PDMM dual-modality optical instructions;
3. The PDMM P-ISA configures the SLM (input/polarization modulation), PD (output/feedback), and UV pump drivers;
4. The SLM generates 3D navigation light patterns under instruction control;
5. Physical hash anchor positioning (PHAT) locks logical coordinates;
6. The recursive self-guiding mechanism drives light propagation or UV cross-locking writing;
7. Dual-modality light wavefield evolution completes native parallel computing, with deterministic operations realized by geometric polarization and thulium ion energy-level computing units;
8. The PD array operates in inference translation or SLM feedback mode, synchronously completing spatiotemporal orthogonal noise screening;
9. The PIC completes final output interpretation or closed-loop correction.

This operation chain represents a paradigm shift: human design intent directly drives physical computing without intermediate digital simulation layers.

A unified three-way closed-loop main control architecture coordinates the operation of the SLM input/rewriting subsystem, UV pump writing/erasure subsystem, and PD feedback/output subsystem. This three-in-one control scheme ensures deterministic synchronization: the SLM encodes light wavefront guidance, polarization regulation and computing logic patterns, the UV pump completes non-volatile refractive index modification and dynamic topological erasure, and the PD array provides real-time light wavefront error and computing result sampling while filtering out orthogonal detector noise.

All three subsystems operate under a shared instruction schedule issued by the PIC, achieving tight coordination between logical programming, physical hardware state

modification, and on-site feedback correction. This collaborative design is critical to maintaining stable light interference, computing repeatability, and runtime reconfigurability in practical working environments.

### 2.1 Physical Hash Mapping (PHM)

Physical Hash Mapping establishes a stable corresponding relationship between random light scattering responses and deterministic logical addresses. Its core principles are:

- Material internal disorder is not a computing error, but an indexable physical computing resource;
- Each chip has a unique PHAT, so consistent logical computing behavior can be achieved despite material differences.

This design breaks the dependence of optical computing on ultra-high-precision uniform material manufacturing.

### 2.2 Three-Layer Mechanism of Physical Hash Addressing

PHAT works across three interconnected layers: physical layer, address layer, and logical layer.

#### 2.2.1 Physical Layer: Intrinsic Response Sampling

- The SLM array emits orthogonal calibration light fields with controllable polarization states;
- Detectors record light scattering, polarization state and interference output signals;
- Rare-earth phase lattices generate high-contrast backward reflection signals, forming a unique optical fingerprint for each chip.

#### 2.2.2 Address Layer: Spatial Hashing of Responses

- Phase lattice positions act as natural physical anchors;
- Continuous light fields are discretized into stable address entries to form the PHAT;
- Realize the mapping from disordered material space to structured logical address space.

#### 2.2.3 Logical Layer: Dynamic Address-Logic Binding

During computing inference, PHM maps logical operations to the optimal physical light paths:

- The SLM loads light phase distributions and polarization states according to the PHAT;
- Light fields evolve along stable, low-loss physical channels;

- Phase lattices provide local alignment and fuzzy navigation guidance.

2.3 Full-Link Consistency: Encoder-Decoder Symmetry and PHAT Synchronization

This architecture reveals a critical full-link consistency problem: input encoding and PD decoding must follow a unified protocol to convert internal light parallelism into meaningful computing results. This design replaces traditional clock synchronization with phase and address-space mapping synchronization.

2.3.1 Logical Symmetry: Entanglement and Deconstruction

To run large-scale AI models, the input and output must share the same PHAT:

- Input Encoder: Maps digital tensors into SLM wavelength-intensity-polarization patterns, encoding information into 3D energy states matching the internal logical distribution;
- PD Decoder: Interprets light intensity-wavelength-polarization patterns through the PDMM P-ISA, identifying energy-level thresholds and interference peaks as logical results, and automatically filtering out uncorrelated PD thermal noise based on spatiotemporal scale differences.

Without this consistent mapping relationship, optical signals will only be unintelligible coherent noise.

2.3.2 Core Nexus: PHAT Alignment

PHAT acts as both a compiler and a decompiler, ensuring that the light wavefront input at the input end can be correctly decoded at the output end, forming a logical closed loop for the entire photonic computing pipeline.

2.4 SugarCube Carrier Concept

"SugarCube" refers to the initial cubic experimental form of the architecture. The architecture natively supports arbitrary 3D geometric shapes, including spheres, hemispheres, irregular volumes, and dendritic structures, fully utilizing the parallel computing advantages of continuous-wave light.

2.5 EDA-Based System Co-Design and Modeling Framework

The B³D-HPA architecture adopts a structured optoelectronic collaborative design process compatible with mainstream electronic and photonic EDA tools. The system is formally divided into two independently analyzable parts:

1. Silicon control subsystem: Including SLM driving logic, UV pump modulation circuits, and PD signal acquisition modules. Traditional digital and analog EDA methods can be

directly used for timing analysis, signal synchronization, power stability, and crosstalk evaluation;
2. Static photonic medium model: The fused silica or sapphire substrate is modeled as a geometrically defined optical material with uniform thermo-optical response and embedded rare-earth hash anchor coordinates. The distribution of rare-earth ions and corresponding physical hash anchor positions can be easily modeled in EDA without excessive complexity. Material inhomogeneity is characterized as global common-mode disturbance, ensuring consistent and repeatable simulation results.

Within this framework, all core functional behaviors can be accurately modeled: SLM-based light wavefront encoding and polarization modulation, incoherent energy-level gating, 3D logic superposition, virtual waveguide self-focusing, and output intensity distribution at the PD plane with spatiotemporal noise screening. Physical hash addressing and recursive self-guiding mechanisms can also be simulated with numerical consistency.

The entire computing chain—from instruction interpretation by the PIC, to SLM execution, UV pump synchronization, dual-modality light evolution, PD dual-mode response with orthogonal noise separation, to result decoding—can be fully modeled, simulated, and traced in formal engineering environments. All key control sequences, including three-subsystem coordination, parallel physical light wavefront evolution, and UV-based writing/erasure operations, must be fully verified through EDA simulation before physical hardware implementation.

2.6 Substrate Selection: Fused Silica and Sapphire

Unified Spatiotemporal Orthogonality Constraint
To ensure the integrity of the PDMM P-ISA, the system must satisfy the following scale-separation inequality:
$\tau_{P\text{-}Noise} / \tau_{S\text{-}Noise} \ll 1 \quad \text{and} \quad \Lambda_{P\text{-}Noise} / \Lambda_{S\text{-}Noise} \gg 1$

Where $\tau$ denotes the temporal scale and $\Lambda$ denotes the spatial scale. This criterion guarantees that the deterministic skeleton logic (S-Noise dominated) remains protected from environmental PD interference (P-Noise dominated) without active digital filtering.

- Fused silica: Low cost, low light loss, low thermo-optical coefficient, compatible with thulium ion doping and stable energy-level distribution, suitable for large-scale mass production;
- Sapphire: High thermal conductivity, strong environmental resistance, suitable for extreme working environments.

Both materials exhibit global, low-dimensional, common-mode physical responses, supporting stable system operation. In contrast, silicon materials produce high-dimensional disordered disturbances that require complex inverse scattering

calculations and introduce additional computing overhead.

Optional pre-doping can introduce compensation agents with opposite thermo-optical coefficients to optimize material physical properties and light writing efficiency, which is selectable according to application scenarios.

## 3 Recursive Physical Logic Probing (A*-based Self-Guiding Writing Mechanism)

### 3.1 Physical Mapping of Heuristic Optimization

The A*-based self-guiding mechanism abandons traditional coordinate-based path search and is redefined as physical logic probing and energy-level trapping:

- Exploration stage: Fuzzy phase scanning performs probabilistic regional navigation within controllable physical tolerance ranges;
- Evaluation stage: PD feedback checks whether the thulium ion energy-level response and polarization state match human-defined logical requirements, and distinguishes effective thulium ion signals from PD noise through spatiotemporal scale differences;
- Locking stage: Effective nodes are solidified into energy-level traps through UV cold writing, forming virtual waveguide segments.

The optimal light path is formed in one step through physical probing and constructive light interference, replacing thousands of digital iterative calculations. Each light wavefront component acts as an independent concurrent computing thread, exploring multiple topological branches in natural parallelism. Existing energy-level traps form physical potential barriers, enabling autonomous path avoidance without explicit software routing.

UV cold writing creates 3D GRIN virtual waveguides. According to Effective Medium Theory, rare-earth ions form a uniform optical medium, realizing boundaryless waveguides without sidewall light loss. The near-parabolic refractive index distribution produces a self-focusing effect, confining light to achieve low-loss, high-density light transmission.

At waveguide intersections, mode coupling and superposition occur. Optimal paths concentrate light energy into strong output peaks, completing physical wavefield collapse. External light beams realize nanosecond-scale dynamic reconfiguration, supporting on-site learning and hardware evolution.

Weight adjustment relies on evanescent coupling between waveguides. UV-tuned refractive index changes control the photon transfer ratio, encoding synaptic weights. Short-term plasticity uses metastable energy levels, while long-term plasticity uses deep energy locking.

The GRIN virtual waveguide achieves single-mode light transmission accuracy with micron-scale robustness, avoiding the trade-off between crosstalk and mode dispersion in silicon waveguides. It realizes pure single-mode transmission, low crosstalk, and high-density layout in 3D space.

At computing nodes, light fields undergo coherent superposition and collapse, naturally realizing weighted summation and activation functions with ultra-low energy consumption.

### 3.2 Relative Phase Difference: Fuzzy Navigation Invariance

The relative phase difference is only used for bounded fuzzy navigation and AI probabilistic computing instructions, not global precise deterministic computing. It maintains spatial correlation within a limited range, supporting probabilistic light wavefield guidance without absolute phase locking. This design realizes low-overhead path exploration while avoiding the instability of coherent phase architectures.

### 3.3 Interference Selection Mechanism

- Low phase difference path → constructive light interference → strong light intensity peak;
- High phase difference path → destructive light interference → weak light intensity.

The output light intensity directly encodes computing solutions without complex post-processing.

### 3.4 Local Phase Anchoring and Regional Stability

Phase lattices provide local temporary phase constraints to limit fuzzy light wavefield exploration within the target space, preventing global divergence. They are not used as high-precision global references, but as spatial boundary references for physical probing.

### 3.5 Heuristic Acceleration & Deep-Write SNR Enhancement

To support real-time 3D anchor positioning, the PIC integrates a dedicated heuristic accelerator at the hardware layer. This module directly performs parallel cost estimation and adaptive path evaluation for recursive optimization, eliminating excessive computing overhead and realizing high-speed, low-delay path planning during 3D optical writing. By executing heuristic reasoning directly in the photonic domain, the system maintains precise position control without sacrificing writing speed or stability.

For deep-volume writing in fused silica, the reflected self-guiding signals naturally weaken with increasing depth. To maintain reliable feedback and consistent positioning accuracy, the architecture uses the nonlinear characteristics of multi-photon excitation to

enhance the reflected signal amplitude and improve the signal-to-noise ratio. This nonlinear enhancement compensates for depth-dependent signal attenuation, ensuring stable self-aligned writing in the entire 3D photonic lattice. Combined with closed-loop calibration and spatiotemporal orthogonal noise screening, the system maintains stable performance even in deep, high-density 3D areas.

## 4 PDMM Physical Dual-Modality Instruction Set Primitives

### 4.1 Deterministic Low-Level Primitives (Iron Skeleton)

PD_ADD(SrcA, SrcB, Dest) → Realized by Geometric Polarization Adder / Thulium Ion Energy-Level Adder
PD_SUB(Minuend, Subtrahend, Dest) → Realized by Geometric Polarization Subtractor / Thulium Ion Energy-Level Competition Gain Subtractor
PD_MUL(Signal, Gain_Factor)
PD_DIV(Signal, Attenuation_Factor)
PD_AND(InA, InB, Out)
PD_OR(InA, InB, Out)
PD_NOT(In, Out)
SLM_WRITE(X,Y,Z,Value)
SLM_ERASE(X,Y,Z)
SLM_READ(X,Y,Z)
PD_OUT(Channel_ID)

### 4.2 Chaotic High-Level Primitives (Semantic Flow, AI-Oriented Probabilistic Computing)

PHASE_FUZZY_COMPUTE(Tensor_Input)
SEMANTIC_BLUR(Entropy_Factor)
COHERENT_EVOLVE(Path_Constraint)
STOCHASTIC_SAMPLING

### 4.3 Modality Synergy & Alignment Primitives

PD_ALIGN_NORM(Chaotic_Field, Logic_Mask, Out)
PD_RESONANCE_LOCK
PD_NOISE_ORTHO_SCREEN(Spatiotemporal_Window, Anchor_Topology, Clean_Signal)
PD_LOGIT_COLLAPSE(Threshold)

### 4.4 PDMM Instruction Priority Hierarchy

- Level 0: Intensity-gated deterministic logic (geometric polarization/energy-level computing, highest robustness)
- Level 1: 3D energy-level arithmetic operations
- Level 2: Chaotic phase semantics and AI high-dimensional parallel probabilistic

computing
- Level 3: Spatiotemporal orthogonal noise screening (auxiliary stability guarantee)

## 5 Core Mechanisms of Physical Hash Addressing (PHAT)

### 5.1 3D Refractive Index Grid Preparation and Multi-Mode Writing Processes

UV dual-wavelength pumping realizes cold writing and erasure without femtosecond laser ablation, supporting repeated reconfiguration and low-damage reusable phase lattice grids. The architecture integrates three complementary writing modes and three erasability levels, forming a complete and scalable engineering manufacturing system.

#### 5.1.1 Point-by-Point Writing: Laboratory-Grade Physical Sovereign Calibration

Point-by-point writing uses high-precision SLMs to adjust the refractive index and polarization response of each voxel like embroidery, with each phase change optimized through hash tables. This establishes the "physical sovereignty" of the architecture, calibrating core logic units and verifying key physical parameters of polarization and thulium ion energy-level computing. Although time-consuming, it defines the maximum precision limit of the architecture.

#### 5.1.2 Depth-Progressive Writing: Industrial Dynamic Growth Process

Depth-progressive writing uses lateral scanning light lines (optical blades) for layer-by-layer material activation, synchronized with vertical infrared SLMs. It supports adaptive "write-inspect-compensate" calibration, balancing precision and speed, serving as the core method for high-throughput mass production of chips and solving yield problems in complex 3D structures.

#### 5.1.3 Single-Shot Full-Layer Writing: Mass-Producible Inclusive Computing Solution

Single-shot full-layer writing uses lateral UV area light sources for global layer activation, synchronized with vertical SLMs to complete full-stack writing in one step. It converts microphysical light writing into a macro "photocopying" process, setting the foundation for large-scale mass production and realizing copy-machine-level scalability of photonic chips.

#### 5.1.4 Cross Hybrid Writing: Industrial Holographic Printing System

The architecture introduces a cross hybrid writing scheme as the ultimate manufacturing solution, integrating all three writing modes in one device to form an industrial holographic printer:

- Vertical axis area light sources / tomographic scanning: quickly complete 90% of the

basic weighting logic in parallel;
- Lateral axis parallel SLM UV arrays: refine residual errors plane by plane after coarse writing;
- Cross-locking addressing: orthogonal light paths form high-contrast energy lattices matched with thulium ion energy levels.

5.1.5 Cross Intersection Writing

Deterministic cross intersection writing creates stable waveguide intersections and computing nodes, which can be pre-simulated in EDA using relative polarization superposition and energy-level competition models.

5.1.6 Dynamic Embodied Evolution Levels (Optional for AGI Only, Disabled in GPU Mode)

This architecture abandons the traditional concept of permanent non-erasable physical structures and provides an optional reconfigurable evolutionary mode only for next-generation photonic AGI embodied intelligence scenarios.

For GPU-equivalent general-purpose photonic acceleration applications, the bone-skin decoupling mechanism is completely disabled, and the chip uses a stable fixed or traditional reconfigurable topology. Manufacturers can freely choose whether to enable this mechanism according to target scenarios.

- Dynamic Evolving Bone (AGI Only): Not a fully fixed physical structure, it is a long-cycle low-frequency plastic layer based on deep energy-level locking. It stores environment-adaptive topological structures with a high modification threshold. When the system detects irreversible signal degradation, the AGI core can trigger UV-driven local annealing and structural erasure, and regenerate more stable topological structures through recursive evolution;
- Flexible Skin (AGI Only): Driven by high-frequency UV modulation, it stores fast-updating LLM weights and transient logic, supporting rapid knowledge iteration similar to traditional model training;
- Bone-Skin Feedback Loop (AGI Only): The bone layer provides a stable physical field for the skin layer, while the skin layer feeds back environmental adaptation data to the bone layer. Verified stable weights in the skin layer can be gradually stored in the bone layer as long-term topological knowledge. This loop enables autonomous system stability optimization for second-generation photonic AGI without human intervention;
- Physical Health Lock (AGI Only): If the PD amplitude monitoring detects abnormal light field fluctuations or noise characteristics deviating from spatiotemporal orthogonal rules, bone modification is locked to prevent wrong self-evolution in unstable states.

5.2 Optical Fingerprint Calibration

Each chip has a unique optical fingerprint formed by the rare-earth ion distribution and

polarization response characteristics, supporting PHAT generation, chip anti-counterfeiting, and consistent logical computing behavior.

### 5.3 Runtime Dynamic Mapping and Path Activation

PHAT provides optimal light wavefronts and polarization states to the SLM, realizing self-evolving optical paths and real-time path correction.

### 5.4 Cold Write/Erase Reconfiguration

UV excitation resets metastable energy levels and polarization modulation states, realizing online reconfiguration and FPGA-like photonic hardware functions.

## 6 Dual-Topology Environmental Robustness Mechanism

### 6.1 Deterministic Energy-Level/Polarization Topology

Incoherent light intensity, geometric polarization state and thulium ion energy-level particle number changes are inherently immune to external environmental disturbances, forming a robust core logic skeleton.

### 6.2 Fuzzy Phase Topology

Relative phase difference and local phase anchoring support low-cost regional navigation and AI probabilistic computing within controllable tolerance ranges, avoiding the need for global phase locking.

### 6.3 System-Level Bounded Stability

The dual-modality synergy suppresses common-mode global physical disturbances, and spatiotemporal scale orthogonality completely isolates PD detector noise, ensuring stable system operation in industrial environments without complex real-time compensation algorithms.

## 7 Optoelectronic Interface and Digital Reconstruction Layer

### 7.1 Physical Quantization: From Probabilistic Wavefields to Digital Signals

PD arrays convert optical wavefields into discrete electrical signals through the photoelectric effect, and synchronously complete spatiotemporal orthogonal noise screening during the photoelectric conversion process.

### 7.2 High-Parallel Output and Array Sampling

Large-scale PD arrays capture full computing results in a single exposure, and naturally filter out ps-level high-frequency PD noise through μs-ms time integration.

### 7.3 PHAT Translation and Logical Alignment

PHAT maps raw optical data (intensity, polarization, energy-level state) into structured digital outputs, and filters out uncorrelated nm-μm scale PD noise through Å-level topological correlation matching.

### 7.4 Hybrid Silicon-Photonics Architecture

Heterogeneous computing combining silicon-based control circuits and silica-based optical processing units.

### 7.5 Hybrid Mode: Discrete Timed Logic and Continuous-Wave Computing

Asymmetric hybrid operation combining digital timing control and continuous-wave parallel computing.

### 7.6 Dual-Path Amplitude Monitoring for Physical Health Assessment

A dedicated PD sub-array monitors reference light amplitude independent of computing signals:

- One channel reads computing interference intensity;
- One channel monitors reference anchor amplitude to evaluate the health of the physical light field and verify the effectiveness of spatiotemporal orthogonal noise screening.

Abnormal reference amplitude or noise characteristic deviation triggers a system state warning and locks high-risk operations such as bone topology modification.

## 8 Typical Application: Physical-Light 3D Rendering and Ray Tracing

### 8.1 Fundamental Difference Between GPU and Photonic Computing

GPUs simulate ray tracing through numerical calculations; B³D-HPA realizes direct physical light propagation, with core deterministic computing completed by geometric polarization and thulium ion energy-level units. With energy consumption reduced by 3–4 orders of magnitude compared with silicon FP32 multiply-accumulators, it has decisive industrial advantages.

### 8.2 Physical Ray Tracing Implementation

UV-written refractive index landscapes realize native ray tracing with single-shot frame output.

### 8.3 Zero-Latency Interactive Response

Instantaneous light interference restructuring realizes real-time camera motion response.

### 8.4 Hardware and Power Efficiency

Ultra-low power consumption without requiring massive computing cores or large-capacity VRAM, and additional power savings from physical-layer native noise

screening instead of digital filtering.

## 9 Extended Features: Physical Observability and Optical Storage

### 9.1 Physical-Layer Debug and Interpretability

The architecture has high transparency and debuggability, supporting real-time observation of spatiotemporal noise separation effects and polarization/energy-level computing states.

### 9.2 Derivative: Silica Photonic Solid-State Storage

Rare-earth-doped fused silica can be used as non-volatile optical storage with high capacity, relying on thulium ion energy-level states for data storage.

## 10 Operational Mechanisms and Engineering Properties

### 10.1 Non-Volatile Physical Storage

UV-programmed energy-level and polarization states retain data without power supply.

### 10.2 Defect Adaptation and Anchor Pruning

The system automatically discards weak hash lattices to maintain computing robustness.

### 10.3 Path Rotation and Lifetime Balancing

Equivalent path rotation extends hardware service life.

### 10.4 Physical Uniqueness and Security

Chip-unique optical fingerprints realize hardware authentication.

## 11 Paradigm Shift: Structure Is Model, Propagation Is Computation

In traditional computing systems: Computation = Instruction fetch + Scheduling + Data movement

In B³D-HPA: Computation = Wavefield injection + Natural propagation + Interference emergence + Physical orthogonal noise screening + Polarization/Energy-level deterministic computing

Clock-free, bus-free, cache-free: the von Neumann bottleneck is fundamentally broken.

## 12 Mitigation of Key Engineering Barriers

### 12.1 Dimensionality Reduction and Closed-Loop Control for Inverse Scattering

Avoids high-dimensional inverse scattering calculations through structural design and closed-loop control.

### 12.2 Coherent Signal Extraction in Strong Scattering

Heterodyne mixing and lock-in amplification realize reliable reflected signal extraction.

12.3 Physical State Preservation and All-Cold Dual-Level Self-Healing Architecture
Eliminates femtosecond laser material damage through energy-level locking and self-healing logic.

12.4 PHAT Table Size Control
Sparse coding and compression technologies maintain real-time system performance.

12.5 SLM Bandwidth Demand and Writing Computational Efficiency
Hybrid writing technology minimizes SLM usage and computing overhead.

12.6 Computational Accuracy Assurance
Multi-path voting and error correction mechanisms ensure engineering-level computing accuracy.

12.7 Closed Engineering Design Loop via EDA Methodology
Full system modeling and verification in standard EDA processes before hardware manufacturing.

12.8 Instruction Priority-Based Environmental Robustness
Light intensity/polarization priority ensures core logic stability; graceful degradation mechanism avoids system collapse, with spatiotemporal orthogonal noise screening as an additional physical stability guarantee.

13 Mass-Production Potential
Redefines chip yield based on stable phase lattice detection, using commercial components without EUV lithography equipment. Multi-mode writing and erasability modes support scalable, low-cost manufacturing.

14 Industrial Innovation
Blank substrates enable user-defined local programming, ensuring data sovereignty and building a decentralized computing ecosystem.

15 PDMM P-ISA Security Policy
The architecture provides inherent physical immunity to software injection and side-channel information extraction. Computing logic is integrated into 3D photonic topology, so tampering requires physical damage to the chip. Internal light coherence and polarization state provide self-verification against intrusion, and spatiotemporal noise orthogonality blocks physical side-channel attacks based on PD thermal noise.

16 Instruction Interoperability and Data Bridging Layer

16.1 Strategic Role of Cross-Architecture Interoperability

The long-term industrial popularization of continuous-wave photonic computing depends not only on performance, but also on the ability to integrate with the existing silicon-based software ecosystem. B³D-HPA does not force full replacement of silicon computing, but supports a heterogeneous computing paradigm where silicon systems handle general control flow and logical management, while B³D-HPA undertakes high-dimensional, heavy-computing workloads.

When used as a GPU-class general photonic accelerator, the architecture focuses on high-throughput parallel computing and instruction compatibility;
When used as an AGI core carrier, it further realizes evolutionary bone-skin decoupling on this basis.

Instruction translation and data bridging are core to the industrial value of the architecture, determining whether the industry is willing to develop quartz-based photonic computing chips on a large scale.

16.2 Importance of Instruction Translation and Data Guidance
Each photonic AGI may evolve a unique adaptive architecture to optimize environmental adaptability. Instruction interoperability and data guidance enable the exchange of adaptive frameworks between different chips:

- The SLM input side supports importing binary software codes and adaptive gene frameworks from silicon systems or other photonic AGIs;
- The PD output side supports exporting adaptive topological frameworks and environmental immune genes for the manufacturing and iteration of other photonic AGIs.

This interworking mechanism preserves the inheritance of digital assets and evolutionary experience, which is a key part of the architecture's value.

16.3 The Two Core Approaches to Interoperability

16.3.1 Instruction Translation and Semantic Reconstruction (Bridge Layer)
The main interoperability mechanism is a semantic translation layer that maps the logical intent of silicon-based instructions (x86, ARM, RISC-V) and high-level frameworks (such as PyTorch) into PDMM P-ISA primitives. This is not a simple one-to-one binary instruction translation, but a high-level compiler that completes semantic reconstruction.

- Silicon Intent Extraction: The PIC or a dedicated front-end compiler performs static analysis on binary code, intermediate representations (IR), or high-level model definitions to extract logical operations, tensor shapes, and data dependencies;
- PDMM Mapping: The compiler maps these high-level operations to native PDMM primitives. For example, matrix multiplication is converted into PD_MUL/PD_ADD cascades realized by polarization/energy-level units, graph traversal is mapped to COHERENT_EVOLVE wavefield evolution, and noise processing is converted to

PD_NOISE_ORTHO_SCREEN;
- Unified Control Flow: The silicon host remains the main control terminal, sending instructions to the photonic device through standardized drivers and APIs.

16.3.2 Direct Data Bridging and Workload Offloading
For scenarios that do not require full instruction translation, a lightweight data bridging protocol directly transfers heavy-computing workloads from the silicon host to the B³D-HPA.

- Workload Partitioning: The silicon host identifies tasks suitable for photonic acceleration;
- PHAT-Aligned Data Injection: The host sends data encoded according to PHAT to the photonic chip;
- Result Output: The chip outputs computing results after noise screening, which are converted back into digital signals by the PIC.

16.4 Ecosystem and Developer Guidance
The PDMM P-ISA is an open instruction framework. Third-party developers are encouraged to build compilers, software frameworks, and plug-ins connected to the B³D-HPA hardware, forming an open and scalable industrial ecosystem.

17 Conclusion

B³D-HPA establishes a fully closed, practically manufacturable continuous-wave optical computing architecture centered on bounded fuzzy phase navigation, physical hash addressing, dual-topology complementary robustness, and the complete PDMM dual-modality instruction framework.

As the defining upgrade, the architecture fully adopts the PDMM Physical Dual-Modality Mapping Instruction Set (P-ISA). In the incoherent deterministic instruction subset, it introduces geometric polarization adders and subtractors, as well as thulium ion energy-level adders and competition gain subtractors as core arithmetic units, with their corresponding physical operating formulas rigorously defined. All phase-based deterministic arithmetic operations from previous versions are replaced by geometric polarization arithmetic, and phase manipulation is now exclusively reserved for AI-oriented probabilistic computing instructions, forming a clean separation of functions between deterministic skeleton logic and chaotic semantic flow.

This version fundamentally eliminates the risk of dual-modality instruction set failure caused by PD thermal drift, by leveraging the verified natural spatiotemporal orthogonality between thulium ion-induced topological noise (S-Noise) and PD detector noise (P-Noise). With Å-level spatial and μs-ms temporal scales for S-Noise, and nm-μm spatial and ps-level temporal scales for P-Noise, the two noise sources are fully non-overlapping in the spatiotemporal domain, enabling native physical-layer signal-noise

separation without complex digital filtering.

Compared with conventional silicon FP32 multiply-accumulators, the architecture achieves a 3–4 orders-of-magnitude reduction in energy consumption, offering an irreplaceable efficiency advantage for large-scale AI and HPC workloads. The bone-skin decoupling evolutionary mechanism remains optional: it is disabled in general-purpose photonic accelerator mode for stable, high-throughput fixed-topology operation, and enabled only for autonomous AGI chips to support generational evolution and self-optimization.

With the instruction priority hierarchy, closed-loop PIC-SLM-PD control, multi-mode UV cold writing, and open instruction interoperability, the architecture provides a complete, scalable engineering path from laboratory validation to mass production. By unifying deterministic geometric polarization/energy-level logic and probabilistic phase-based semantic flow, B³D-HPA lays a robust foundation for the next generation of continuous-wave optical computing.

By mathematically defining geometric polarization as the deterministic arithmetic basis (Jones Matrix Model) and leveraging phase-induced entropy shaping for AI regularization (PES Model), B³D-HPA effectively decouples logical computing from physical environmental noise, providing a formal engineering foundation for industrial photonic AI.

B³D-Lite Physical Mapping Table (V3.53-Lab-Alpha)

PDMM PIC Lite Demo Code
INIT_MEDIUM("Fused_Silica")
SLM_WRITE(0,0,0, LOGIC_1)
SLM_WRITE(10,10,10, LOGIC_1)
PD_ALIGN_NORM(CHAO_MODE, DETERM_MASK, RESULT)
PD_NOISE_ORTHO_SCREEN(US_MS_WINDOW, ATOM_ANCHOR_TOPO, CLEAN_SIGNAL)
PD_LOGIT_COLLAPSE(THRESHOLD)
PD_OUT(CHANNEL_MAIN)
MONITOR_REF_AMPLITUDE()

PDMM P-ISA Mapping Table
PD_ADD | Incoherent intensity summation | Volumetric population inversion | Natural perturbation immunity
PD_SUB | Gain competition subtraction | Cross-relaxation depletion | Precise intensity difference control
PD_MUL | Stimulated emission scaling | Gain-factor amplification | Linear intensity mapping
PD_DIV | Absorption attenuation | Attenuation-factor scaling | Linear intensity mapping
PD_AND / PD_OR / PD_NOT | Threshold-gated volumetric logic | Spatial intersection of excited states | 3D gate parallelism

PD_ALIGN_NORM | Chaotic field filtering | Deterministic skeleton masking | Semantic stability
PD_NOISE_ORTHO_SCREEN | Spatiotemporal scale screening | Physical orthogonal projection | PD thermal drift immunity
PD_LOGIT_COLLAPSE | Probability-to-logit conversion | Intensity thresholding | AGI output control